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IN THE CLAIMS:

- 1 1.(previously presented) A backplane system to connect in common a plurality
2 of peripheral computing devices each on an individual daughter card such that
3 there is a corresponding number of daughter cards, wherein the daughter cards
4 are configured as cPCI-compliant cards each having a slot connector, the back-
5 plane system comprising:
6 a backplane bus having a plurality of slots for receiving one or more
7 of the cPCI-compliant cards, wherein said slots are spaced from one another at a
8 pitch to minimize impedance mismatching, each slot including a card connector;
9 and
10 an interposer card for each daughter card, said interposer card in-
11 cluding means to connect to the slot connector and to said card connector such
12 that said interposer card is interposed between the daughter card and a slot of
13 said plurality of slots of said backplane bus, wherein said interposer card is con-
14 structed to reduce the reflective wave path from the daughter card to the inter-
15 poser card, thereby reducing the impedance mismatch and thereby allowing the
16 noise to settle in time for the interposer card to output, in response to receiving a
17 reflective wave, an incident wave switching at said slot connector.
- 1 2. (original) The backplane system as claimed in **Claim 1** wherein said back-
2 plane bus is a cPCI backplane, the system further comprising a cPCI interface
3 coupled between said backplane bus and the daughter cards, wherein said inter-
4 poser card is couplable between said cPCI interface and said slot connector of
5 said backplane bus.
- 1 3.(original). The backplane system as claimed in **Claim 2** wherein said cPCI
2 interface includes a state machine to regulate timing, direction and enablement
3 associated with operation of said interposer card.

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- 1 4.(original). The backplane system as claimed in Claim 3 wherein said state
2 machine and said interposer card are implemented integrally with said interface.
- 1 5.(original). The backplane system as claimed in Claim 1 wherein said interposer
2 card includes a GTLP transceiver to produce incident wave switching.
- 1 6.(original). The backplane system as claimed in Claim 1 wherein said back-
2 plane bus has an impedance of about 65 ohms.
- 1 7.(original). The backplane system as claimed in Claim 1 wherein said back-
2 plane bus further includes impedance terminations at opposing ends thereof.
- 1 8.(original). The backplane system as claimed in Claim 7 wherein each of said
2 impedance terminations of said backplane has an impedance of about 40 ohms.
- 1 9.(original). The backplane system as claimed in Claim 1 wherein each of said
2 slots includes a stub connector having a stub impedance of about 50 ohms.
- 1 10.(original) The backplane system as claimed in Claim 1 wherein said back-
2 plane bus includes 21 of said plurality of slots.
- 1 11.(previously presented) A method of increasing the throughput of a conven-
2 tional cPCI-compliant backplane architecture having a plurality of slots coupled to
3 a common backplane bus for receiving one or more cPCI-compliant daughter cards,
4 the method comprising the step of inserting an interposer card between each of
5 the daughter cards and its corresponding slot, wherein said interposer card in-
6 cludes means for reducing the reflective wave path from the daughter card to the
7 interposer card, thereby reducing the impedance mismatch and thereby allowing

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8 the noise to settle in time for the interpose card to output, in response to receiv-
9 ing a reflective wave, an incident wave.

1 12.(currently amended). The method as claimed in **Claim 11** further compris-
2 ing the step of installing at the ends of the backplane bus termination imped-
3 ances each having an ~~30~~ impedance of about 40 ohms.

1 13.(original). The method as claimed in **Claim 11** further comprising the step of
2 forming stub connectors of each of the slots with stub impedances of about 50 ohms.

1 14.(original). The method as claimed in **Claim 11** further comprising the step of
2 coupling said interposer card with a state machine configured to regulate timing,
3 direction, and enablement of said incident-wave switching.

1 15.(original). The method as claimed in **Claim 11** wherein said interposer card
2 includes a GTLP transceiver for generating said incident-wave switching.

1 16.(original). The method as claimed in **Claim 11** wherein said backplane bus
2 has an impedance of about 65 ohms.

1 17.(original). The method as claimed in **Claim 11** further comprising the step of
2 latching the signal transmissions associated with said incident-wave switching so
3 as to control the signal propagation to and from the backplane bus.

1 18.(original). The method as claimed in **Claim 11** wherein the backplane bus is a
2 cPCI backplane and one or more of the daughter cards is a cPCI-compliant card, further
3 comprising the step of interposing between the cPCI-compliant card and the inter-
4 poser card a cPCI interface.

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1 19.(original). The method as claimed in Claim 18 further comprising a state ma-
2 chine formed integrally with said interface, wherein said state machine regulates
3 operation of said interposer card.

1 20.(original). The method as claimed in Claim 18 further comprising a state machine
2 formed integrally with said interface, wherein said state machine regulates operation of
3 said interposer card, further comprising the step of forming said interposer card inte-
4 grally with said interface.